REMARKS

Applicants respectfully request the Examiner's reconsideration of the present application as amended.

Claims 1-71 are pending in the present application.

Claims 6-7, 10-13, 15-17, 21, 23-25, 27-28, 32-44, 61, and 65-71 are objected to because of informalities.

Claims 1-4, 8, 12-16, 18-24, 26-29, 34, 39-44, 46-47, 53-62, 65, and 68-71 are rejected under 35 U.S.C. §102(b) as being unpatentable over U.S. Patent 5,659,484 ("Bennett").

Claims 5-7, 9-11, 17, 25, 30-33, 35-38, 63-64, 66-67 are rejected under 35 U.S.C. §103(a) as being unpatentable over Bennett in view of U.S. Patent 5,521,837 ("Frankle").

Claims 45, and 48-52 are rejected under 35 U.S.C. §103(a) as being unpatentable over Bennett in view of U.S. Patent 5,541,849 ("Rostoker").

Claims 1-14, 18-22, 43, and 70-71 have been canceled.

Claims 15-17, 23, 25-28, 32-33, 37-38, 41-42, 44, 59 and 68-69 have been amended.

Claims 72 and 73 have been added.

Support for the new and amended claims is found on pages 4-28 of the specification, Figures 1-8(k) of the drawings, and claims 1-71 as originally filed. No new matter has been added.

Claims 6-7, 10-13, 15-17, 21, 23-25, 27-28, 32-44, 61, and 65-71 are objected to because of informalities.

Claims 15-17, 23, 25-28, 32-33, 37-38, 41-42, 44, 59 and 68-69 have been amended according to the suggestion provided by the Examiner.

Applicants submit that the term "slack" as used with reference to positive and negative slack, may be used as both the singular and plural form. Applicants thus submit that the use of the term "slack" in claims 15, 16, 23-25, and 61-65 is appropriate.

Applicants submit that in view of the amendment to claims 15-17, 23, 25-28, 32-33, 37-38, 41-42, 44, 59 and 68-69 and the explanation above, the objections to claims have been overcome.

The Examiner has rejected claims 1-71 under 35 U.S.C. §102(b) and §103(a) as being unpatentable over Bennett, Frankle, and Rostoker. In particular, the Examiner has stated that

> As per claims 1, 18, 26, 59, 70-71, the short path and long path timing constraints are described in col. 13, line 5 to col. 14, line 2, wherein at least the PERIOD, FREQUENCY, MAXDELAY, MAXSKEW, and OFFSET constraints correspond to the long path timing constraints (see Applicant's specification, page 9, lines 20-21 and page 1, lines 16-19), and wherein at least the OFFSET/BEFORE, OFFSET IN/AFTER. OFFSET OUT/AFTER, OFFSET OUT/BEFORE. And BLOCK constraints correspond to the short-path timing constraints (see Applicant's specification, page 9, lines 21-23); wherein the minimum and maximum delay budgets generated based on these timing constraints are further described in col. 18, line 1 to col. 19, line 61; and wherein such designing of the system based on the minimum/maximum delay budgets are part of the placement and routing algorithms used which applied these delay budgets (see col. 26, line 53 to col. 30, line 20; see also col. 10, line 48 to col. 11, line 32)

(2/23/2006 Office Action, pp. 5-6)

As stated above, claims 15-17, 23, 25-28, 32-33, 37-38, 41-42, 44, 59 and 68-69 have been amended. New claims 72-73 have been added.

It is submitted that Bennett, Frankle, and Rostoker do not render claims 15-17, and 23-42, 44-69, and 72-73 unpatentable under 35 U.S.C. §102(b) and §103(a).

Bennett includes a disclosure of a device independent, frequency driven layout system and method for field programmable gate arrays ("FPGA") which allow for a circuit designer to specify the desired operating frequencies of clock signals in a given design to the automatic layout system to generate, if possible, a physical FPGA layout which will allow the targeted FPGA device to operate at the specified frequencies.

Actual net, path and skew requirements are automatically generated and fed to the place and route tools. The system and method of the present invention evaluates the frequency constraints, determines what delay ranges are acceptable for each electrical connection and targets those ranges throughout the layout. (see Bennett Abstract).

Frankle includes a disclosure of suggested delay limits for use by layout tools which cause a programmable integrated circuit device to implement a logic design. The suggested delay limits can be used by such tools as an initial placement algorithm, a placement improvement algorithm, and a routing algorithm for evaluating and guiding potential layouts. The suggested delay limits take into account characteristics of the programmable device being used by estimating lower bound delays for each connection in a logic design, and take into account any previously achieved delays or achievable delays for each connection in calculating the suggested limits. Results of routing benchmark designs using the novel suggested limits show improved timing performance for all benchmark cases tested. (see Frankle Abstract).

Rostoker includes a disclosure of a methodology for generating structural descriptions of complex digital devices from high-level descriptions and specifications. The methodology uses a systematic technique to map and enforce consistency of the semantics imbedded in the intent of the original, high-level descriptions. The design activity is essentially a series of transformations operating upon various levels of design representations. At each level, the intended meaning (semantics) and formal software manipulations are captured to derive a more detailed level describing hardware meeting the design goals. Features of the methodology include: capturing the users concepts, intent, specification, descriptions, constraints and trade-offs; architectural partitioning; what-if analysis at a high level; sizing estimation; timing estimation; architectural trade-off; conceptual design with implementation estimation; and timing closure. The methodology includes using estimators, based on data gathered over a number of realized

designs, for partitioning and evaluating a design prior to logic synthesis. From the structural description, a physical implementation of the device is readily realized. Techniques are provided for estimating design performance, from behavioral/functional descriptions. Given a behavioral or a block diagram description of data flow in a design, pin-to-pin timing and minimum clock cycle for the design can be estimated accurately. An RTL description may thus be synthesized from a behavioral description such that timing constraints imposed at the behavioral level are achieved. The timing of a synthesized design is estimated, and the design is re-synthesized until a design is arrived at that meets timing constraints imposed at a higher level. (See Rostoker Abstract).

It is submitted that Bennett, Frankel, and Rostoker do not teach or suggest generating minimum delay budgets for connections from short-path timing constraints, wherein generating the minimum delay budgets for connections comprises allocation of positive and negative slack using successive-over-relaxation where more slack than is available is allocated.

On the contrary, Bennet discloses a connection relaxation technique where only slack which is available is allocated (col. 19, line 66 to col. 20, line 5). Bennet provides a pseudocode representation of the Relax Connection Targets process (col. 21, lines 5-65). The pseudocode illustrates that only available slack is re-distributed to connections and that slack allocation never exceeds the target. Bennett determines the amount of connection delay that is available for a path by adding the actual connection delay to the slack values. If other paths cause a connection along this path to be reduced further than this path's original connection target, additional slack will be available to other connections in this path, relative to the exiting connection target. It is this available slack that is re-distributed (col. 21, lines 23-45).

Frankle only discloses a timing driven method for laying out a user's circuit onto a programmable integrated circuit device.

Rostoker only discloses a method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including estimation and comparison of timing parameters.

In contrast, amended claim 15 as amended states

> A method for designing a system, comprising:
> generating minimum delay budgets for connections from short-path timing constraints, wherein generating the minimum delay budgets for connections comprises allocation of positive and negative slack using successive-over-relaxation where more slack than is available is allocated; and
> designing the system in response to the minimum delay budgets.

(Claim 15 as amended) (Emphasis added).

Claims 23 as amended, includes the similar limitations of using successive-over-relaxation where more slack than is available allocated. Given that claims 16-17, and 24-25 depend from claims 15 and 23 as amended, it is likewise submitted that claims 16-17 and 24-25 are also patentable under 35 U.S.C. §102(b) and §103(a) over Bennett, Frankle, and Rostoker.

It is submitted that Bennett, Frankle, and Rostoker do not teach or suggest generating minimum and maximum delay budgets for connections from long-path and short-path timing constraints, wherein for each connection the minimum and maximum delay budgets are determined such that at least one of the minimum delay budgets and maximum delay budgets is determined with consideration of the other.

On the contrary, Bennett discloses computation of minimum delay targets (mintarget/con.mintarget) and maximum delay targets (maxtarget/conn.maxtarget) that are computed independently of each other. Bennett provides a pseudocode representation of the Compute Connection Target process used (col. 19, lines 31-61). The pseudocode illustrates that maxtarget is computed from the values maxslack, path.numconns, conn.delay, and sumdelay. The pseudocode illustrates that mintarget is

computed from the values minslack, path.numconns, conn.delay, sumdelay, minslack (col. 19, lines 44-47, lines 49-54, lines 56-61). The variables maxtarget and mintarget are computed independently and without consideration of each other.

Frankle only discloses a timing driven method for laying out a user's circuit onto a programmable integrated circuit device.

Rostoker only discloses a method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including estimation and comparison of timing parameters.

In contrast, amended claim 26 states

> A method for designing a system, comprising:
> generating minimum and maximum delay budgets for connections from long-path and short-path timing constraints, wherein for each connection the minimum and maximum delay budgets are determined such that at least one of the minimum delay budgets and maximum delay budgets is determined with consideration of the other; and
> designing the system in response to the minimum and maximum delay budgets.

(Claim 26, as Amended) (Emphasis added).

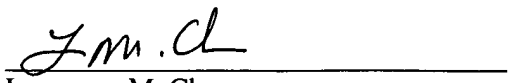
Claim 59 includes similar limitations. Given that claims 27-42, 44-58, and 72-73 depend directly or indirectly from claim 26 and claims 60-69 depend directly or indirectly from claim 59, it is likewise submitted that claims 27-42, 44-58, 72-73, and 60-69 are also patentable under 35 U.S.C. §102(b) and §103(a) over Bennett, Frankle, and Rostoker

In view of the amendments and arguments set forth herein, it is respectfully submitted that the applicable rejections and have been overcome. Accordingly, it is respectfully submitted that claims 15-17, 23-42, and 44-69, as amended, and new claims 72-73 should be found to be in condition for allowance.

If any additional fee is required, please charge Deposit Account No. 50-1624.

Respectfully submitted,

Dated: May 19, 2006



Lawrence M. Cho
Attorney for Applicant
Registration No. 39,942

P.O. Box 2144
Champaign, IL 61825
(217) 377-2500